Firmware Control of Block IV Ranging Demodulator Assembly

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The Mark III Data System Development Plan is encouraging engineers designing equipment for use in the Deep Space Network to utilize computer control and monitoring. It is becoming apparent that the difficulty of development and cost of software are prohibitive. A concept called firmware is proposed. Firmware is a design concept which directs the engineer to employ special-purpose digital and/or analog circuitry whenever possible to reduce software or interface requirements. The Ranging Demodulator Assembly (RDA) is being developed under the firmware concept. By employing firmware, the RDA interface and software requirements have been kept to a minimum. The phase calibration of the RDA is achieved with a single switch or one-line command from the computer. Monitoring is handled by the firmware which supplies one line to the computer indicating the operability of the RDA.

I. Introduction

The Mark III Data System Development Plan (DSDP) is encouraging engineers designing equipment for use in the Deep Space Network to utilize computer control and monitoring. It is tempting for the circuit designers to design and build equipment as in the past and simply use the computer as a substitute for man. This approach requires the computer to be programmed to perform those operations, both open loop and closed loop, that have been performed manually in the past. It is becoming apparent, however, that the difficulty of development and cost of software are perhaps prohibitive. The Command System, for example, was designed to operate with a symbol rate of one kilobit per second. This machine was built with the idea in mind that the computer would monitor and control all possible functions, and it was subsequently found that under computer operation the symbol rate was reduced to a maximum of 1.6 bits per second. The limitations were due to the number of operations imposed upon the computer to perform in real time. Our observations lead us to two conclusions concerning computer-controlled hardware:

(1) Computer-controlled hardware should be designed and built to minimize the number of functions to be controlled and monitored by the machine.

(2) Software to control computer-controlled hardware should be kept to a minimum by judicious design of the hardware to be controlled.

The Block IV Ranging Demodulator Assembly (RDA) is being designed based on these two conclusions.

II. Firmware

Firmware as used here is a system design concept directed toward optimizing the interface between a computer and the hardware it controls. The firmware concept is to employ special-purpose digital and/or analog circuitry whenever possible to reduce software or interface requirements. The circuitry is developed from a flow chart which describes the operations and sequence to be performed. We are employing firmware in both control and monitor applications.

The expense of developing software is reduced by performing repetitive operations with firmware. Software development cost is therefore reduced by the elimination of control and monitor subroutines. Additionally, costs are reduced because the engineer most familiar with the hardware to be controlled is the one developing the control and monitor circuitry.

The use of firmware will save significant time in the real-time operations of the computer since the computer will not have to perform closed-loop operations but will only be required to signal to the firmware to do its special-purpose job. The firmware will flag the computer at the completion of its task. The ensuing time can be utilized by the computer to perform jobs with other pieces of hardware or computational tasks. Computer time will also be economized since the machine will not have to observe a large number of monitor points but will simply monitor a few firmware outputs to determine the total health and operability of the hardware.

There are also advantages due to firmware accruing to manual control. Since the firmware can be used by the controlling computer to perform simple repetitive tasks, it will likewise be available to the man operating the machine or checking out the machine when the computer is not in control. Hence, phase calibration of an RDA will be achieved by the operator depressing a single pushbutton. Another advantage that will accrue to manual control through the use of firmware is the uniformity of the control of the machine. Jobs performed by firmware will always be performed in the same sequence, thereby eliminating any variance due to differences between operators.

With the use of firmware to perform control and monitor operations, there will be a reduction in the complexity of the interface with the computer. There will be, for instance, fewer lines, or points, for the computer to monitor to determine operability. A particular operation involving a control loop will require only one line from the computer since the firmware will handle the control and monitor required to close the loop.

III. Block IV RDA Control Unit

A simplified block diagram of the Ranging Demodulator Assembly is shown in Fig. 1. The firmware may be conveniently divided between that firmware applied to monitor and that firmware applied to control. One example of each of these two categories of firmware is discussed below beginning with monitor firmware.

A. Monitor Firmware

The monitor firmware approach is to compare the control input with the state of the controlled device. If the result disagrees with the control input, an alarm is initiated. This technique is applied wherever possible in a module, and the results are logically combined into one alarm. In the RDA this approach is used to monitor the reference phase shifters and also the input attenuator. Housed within the IF and phase switch module in the RDA is an eight-bit digital attenuator. This attenuator is comprised of eight switched T-pad attenuators under control of a binary weighted word. Shown in Fig. 2 is the attenuator confirmation firmware flow chart. The firmware compares the state of the command line with the condition of the relay and signals an alarm if the two are different. This is repeated for each of the eight attenuator steps. The alarm indicators are then combined into a single line that controls the confirmation lamp on the front panel of the control unit and will also be available to the computer as a monitor of the operational capability of the input attenuator of the RDA.

B. Phase Calibrate Firmware

The 10-MHz signal in the Ranging Demodulator Assembly is coherently detected in the bandpass amplifier and coherent amplitude detector (CAD) module. Phase calibration is achieved when the reference is aligned with the ranging modulation which is equivalent to being orthogonal to the carrier. Figure 3 is a simplified diagram of the coherent amplitude detector and the phase calibrate hardware of the RDA. The scheme employed by the firmware phase control, in very general terms, is to step the control voltage to the linear analog phase shifter by one least-significant bit (LSB) and then, after a suitable delay, to take account of the lowpass delay characteristic of the dc amplifier, to initiate an analog-to-digital (A/D) conversion and observe the most-significant bit

(MSB). When an occurrence of sign change occurs (MSB changes state), the direction of steps into the digital-to-analog converter (D/A) is reversed, and the next step to the linear analog phase shifter will be in the opposite direction. Therefore, if one were to observe the analog control voltage to the phase shifter during a phase calibrate cycle, one would observe that the voltage ramps upward (in LSB steps) until the analog output of the coherent amplitude detector/lowpass amplifier reaches zero, at which time the control voltage would oscillate up and down in increments of one least-significant bit of the D/A converter. The output of the D/A converters will step for approximately 46 seconds (256 counts), which is guaranteed to be adequate to ramp the phase shifters to a null.

The phase calibrate firmware may be examined in more detail by studying Fig. 4, phase calibrate firmware flow chart, and Fig. 5, phase calibrate firmware (which is offered as an aid in understanding the flow chart). A phase calibrate operation may be initiated by either an operator or the computer. Given a request for a phase calibrate cycle from either of these two sources, a start pulse is generated. Without reference to the order in which they occur, the following operations are performed by the start pulse:

(1) The Channel 1 and Channel 0 up/down counter indicated by the position of the SOURCE selector switch (RCV 1, RCV 2, PHASE) on the front panel of the RDA control unit is set to one quarter of its full-scale value. This aspect of the initialization is done in order to guarantee that the final value of the phase angle will not be at one end of the linear region of the phase shifter.

(2) The initial sign (IS) one-shot is enabled.

(3) The clock counter (CC) is cleared. The clearing operation generates the PHASING signal.

The PHASING signal generated in paragraph (3), above, performs a sequence of initializing operations which are enumerated below:

(1) Release the up/down counter gates selected by the SOURCE selector switch so that the control voltage can begin to ramp toward its final value.

(2) Light the PHASE CALIBRATE lamp.

(3) Enable the delay counter (DC) which will be used to delay the up/down count long enough for the MSB/$\overline{\text{MSB}}$ of the A/D converter to reach its final value each cycle.

(4) Start the clock.

The clock pulse performs two operations. It increments the clock counter and initiates an A/D converter start pulse (ADC ST). The ADC ST pulse sets the delay counter to its starting value and also initiates a conversion by both the Channel 0 and Channel 1 A/D converters. If the last increment of the clock counter pushed its sum to final value, then the clock will be halted and the PHASING signal will be inhibited. Since the PHASING signal is used as a gating signal to the up/down counters, the up/down counters will be halted at their present values.

Several cycles of the Channel 0 A/D clock output are counted by the delay counter to generate a delayed clock pulse. In general, the delayed clock pulse is used to increment or decrement the appropriate up/down counters based upon the state of the current most significant bit as compared to the initial sign (sign of output at start of counting). If the initial sign and most significant bit agree, the counters will be incremented, thereby causing the circuitry to seek the null closest to the midrange of the phase shifter. If they disagree, the counter will be decremented. The state of the initial sign is determined after a delay of four delayed clock pulses. The four-count delay is necessary in order to give the lowpass filter in the output of the CAD time to respond to the initial setting of the phase shifter.

Time delay between a clock pulse and an up/down count is approximately 10 microseconds. Hence there is about 180 milliseconds between one count and the next. The above operations are repeated each 180 milliseconds for 256 times, which is sufficient to step the D/A converters through the entire range of the phase shifters. After the cycle is repeated 256 times the CADs are phased to within ± 3 degrees of optimum and the PHASE CALIBRATE indicator is extinguished. The firmware will remember (for both channels) the control voltage required for any SOURCE (RCV 1, RCV 2, PHASE) used during the calibrate cycle. This feature permits the operator/computer to phase calibrate, prior to a mission, RCV 1 and RCV 2 in case receivers need to be changed during the mission.

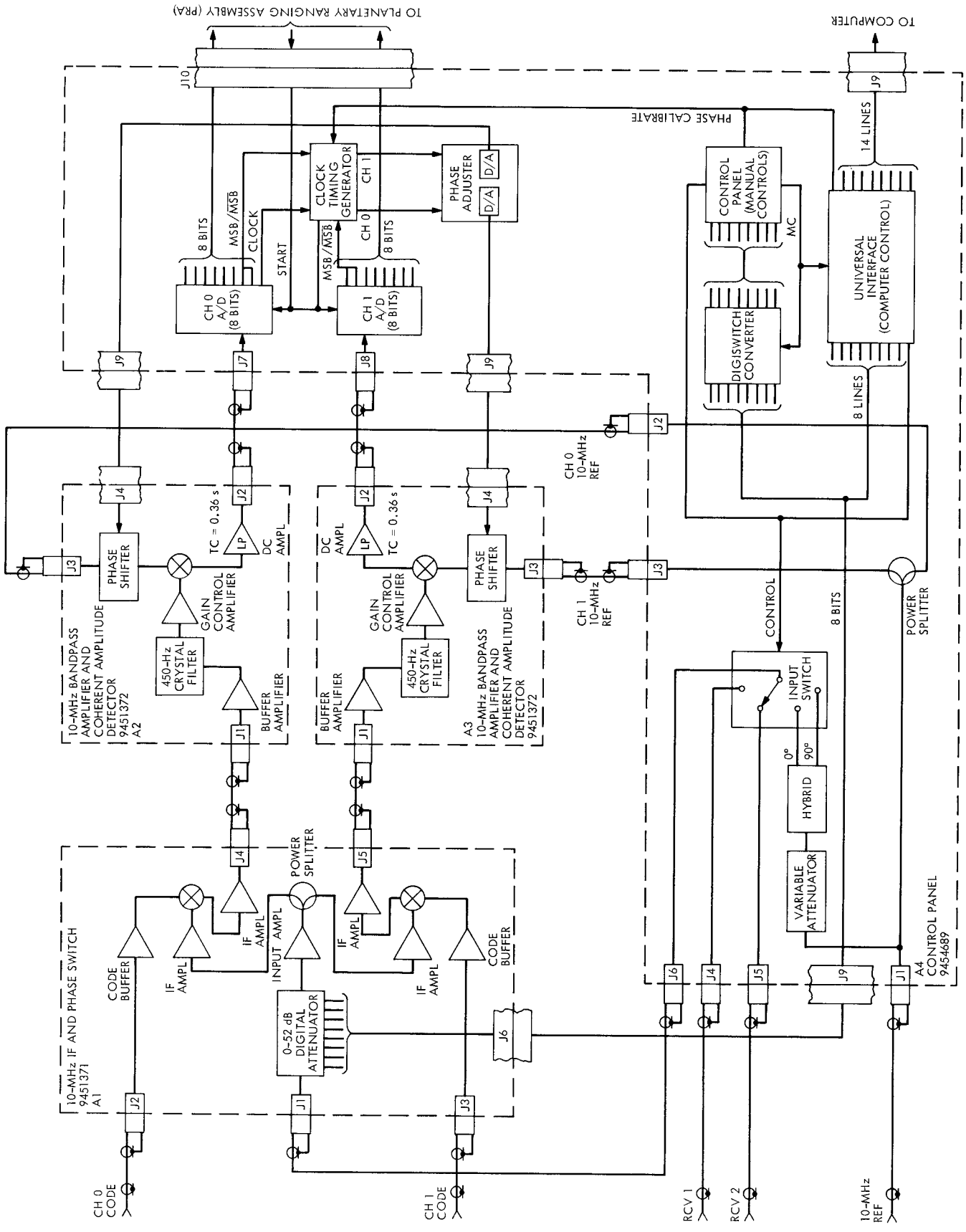

Fig. 1. Functional block diagram of the ranging demodulator assembly

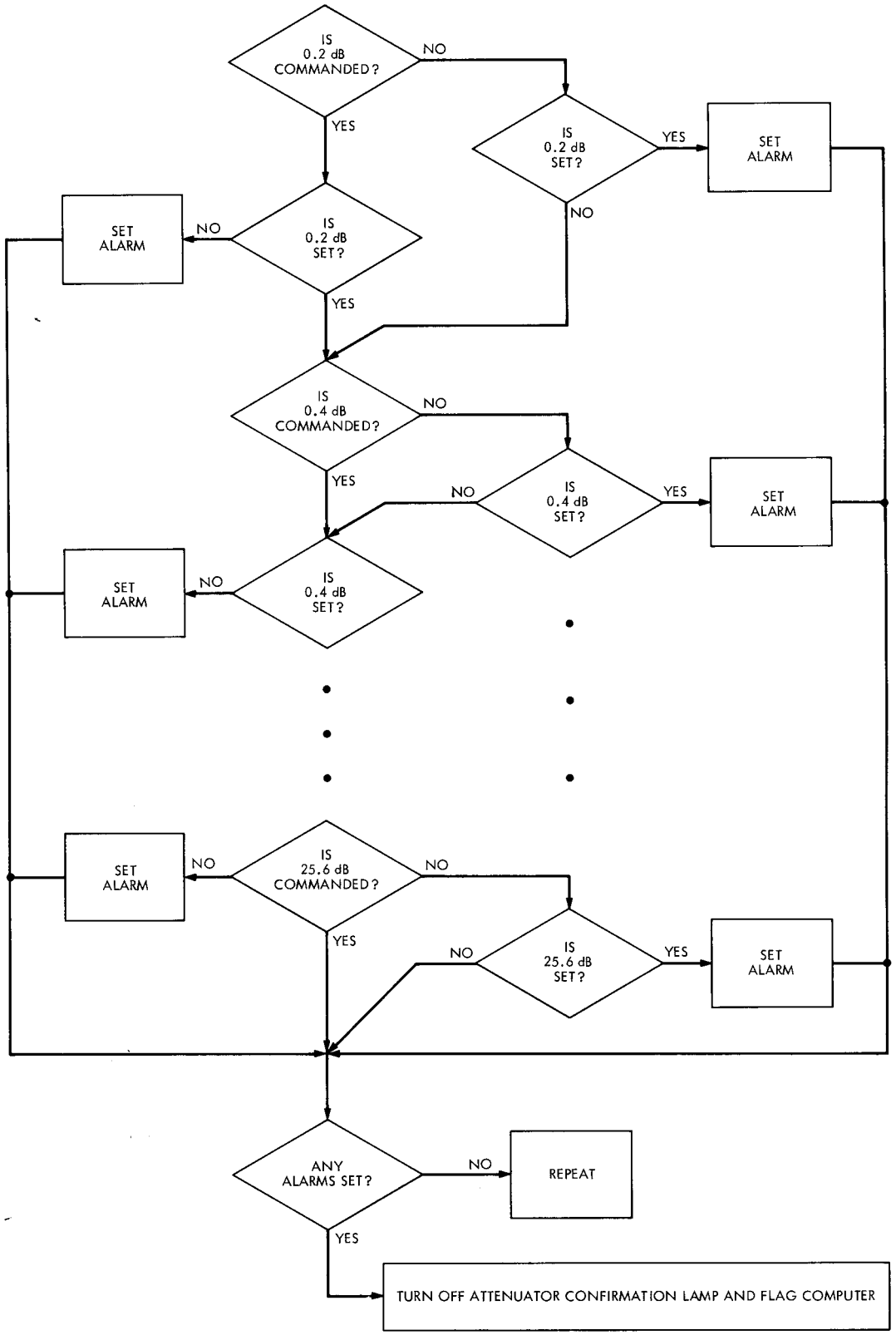

Fig. 2. Attenuator confirmation firmware flow chart

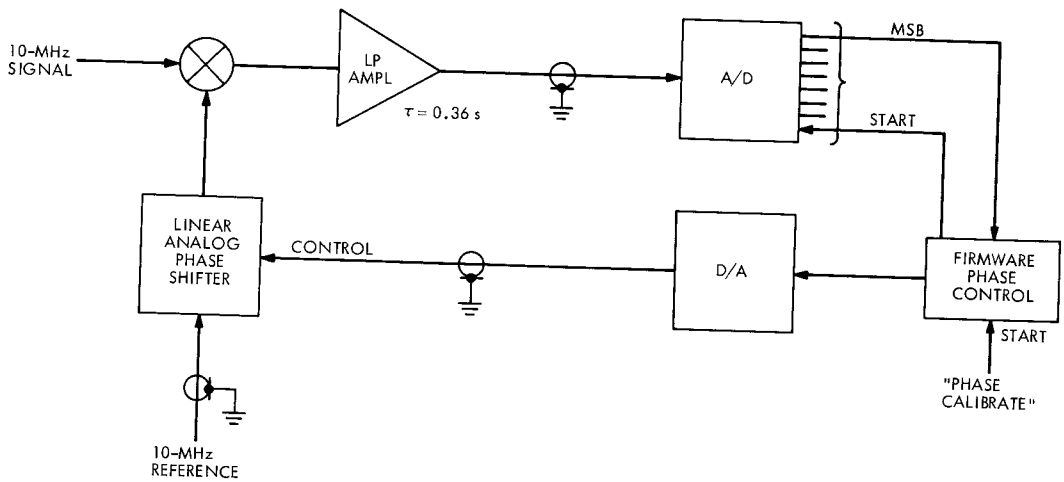

Fig. 3. Coherent amplitude detector

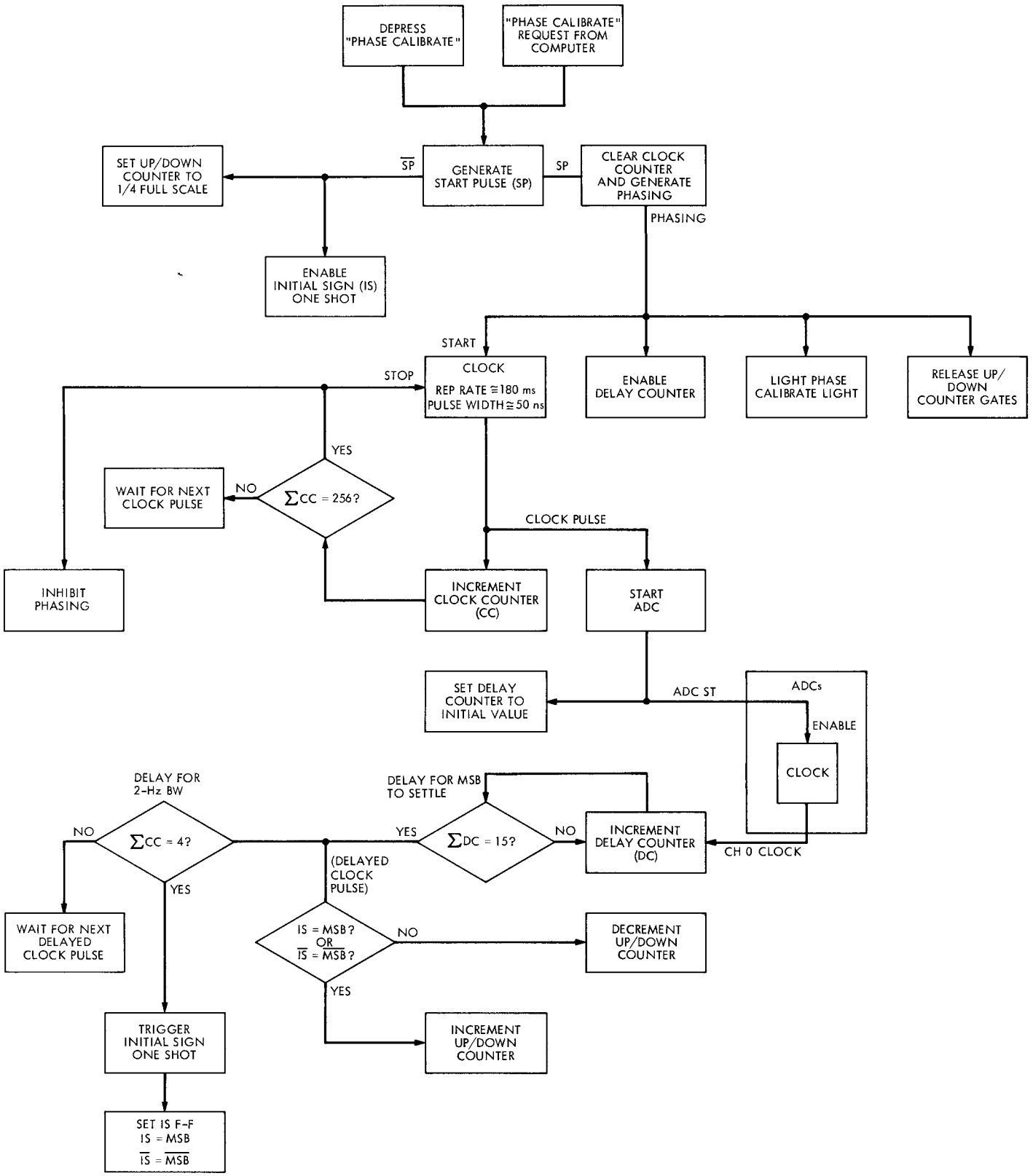

Fig. 4. Phase calibrate firmware flow chart

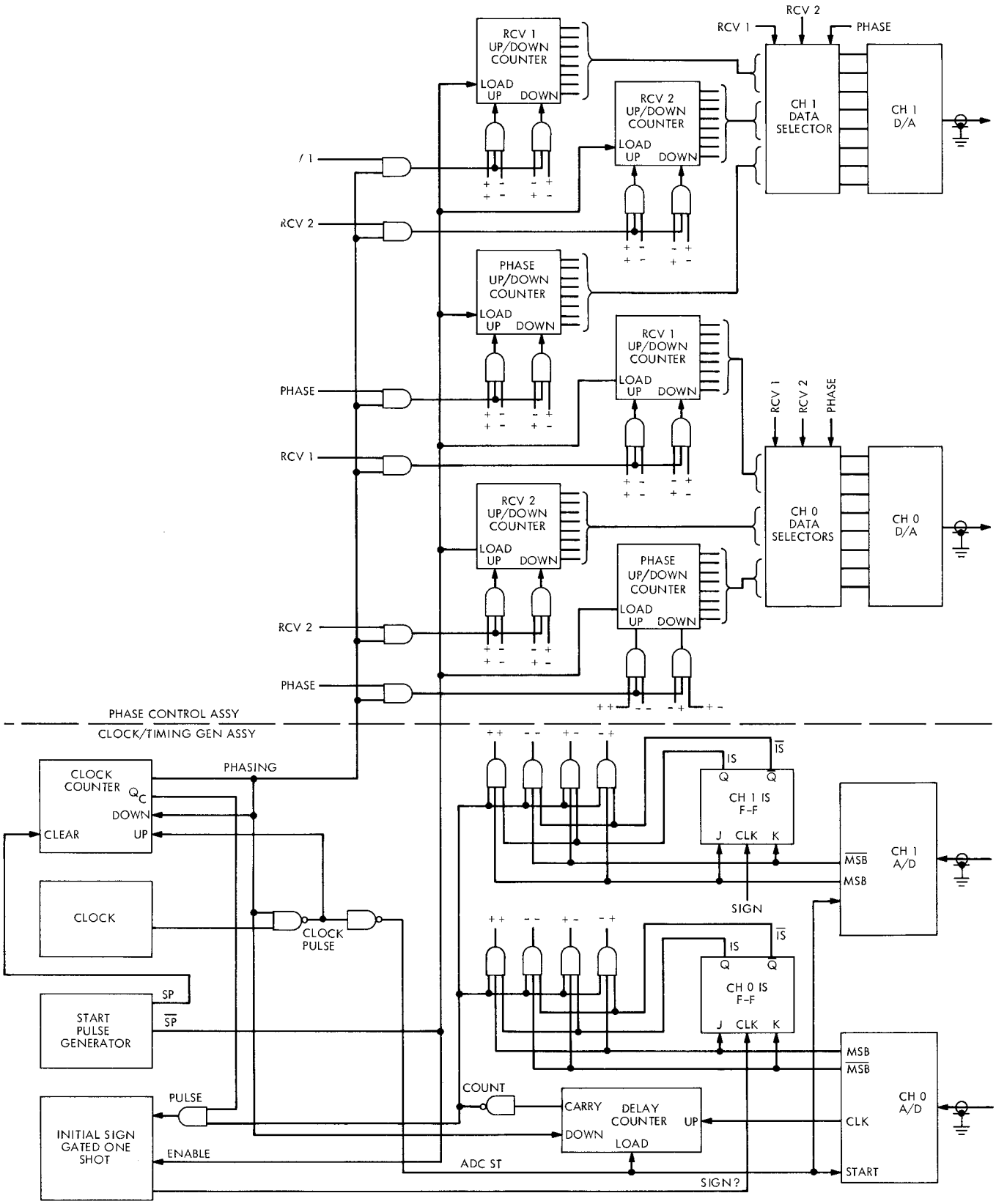

Fig. 5. Phase calibrate firmware